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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	KM1-001
First Inventor or Application Identifier	Keiji Jono
Title	Methods of Forming an Isolation etc.
Express Mail Label No.	EL465686819US

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 36]
(preferred arrangement set forth below)
   - Descriptive title of the Invention Plus title pg.
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 3]
4. Oath or Declaration [Total Pages 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
   (for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
9. [ ] English Translation Document (if applicable)
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [X] Other: ~~Check~~

16. **If a CONTINUING APPLICATION,** check appropriate box, and supply the requisite information below and in a preliminary amendment:
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ______/______
Prior application information: Examiner ______ Group / Art Unit: ______
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17. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label 021567 (Insert Customer No. or Attach bar code label here) or [ ] Correspondence address below

Name	Frederick M. Fliegel, Ph.D.				
	Wells, St. John, Roberts, Gregory & Matkin P.S.				
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Name (Print/Type)	Frederick M. Fliegel, Ph.D.	Registration No. (Attorney/Agent)	36,138
Signature	[signature]	Date	Aug 31, 2000

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 1,740.00

Complete if Known	
Application Number	Filed Herewith
Filing Date	Filed Herewith
First Named Inventor	Keiji Jono et al.
Examiner Name	Unknown
Group / Art Unit	Unknown
Attorney Docket No.	KM1-001

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 23-0925

Deposit Account Name: Wells, St. John et al.

[X] Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. [X] Payment Enclosed:
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	690
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	61	-20** =	41	X	18	=	738
Independent Claims	7	- 3** =	4	X	78	=	312
Multiple Dependent						=	

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 1,050.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	690	249	345	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) ____________________

Other fee (specify) ____________________

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0

SUBMITTED BY

Complete *(if applicable)*

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EL465686819

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and

belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

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EL465686819

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

METHODS OF FORMING AN ISOLATION TRENCH IN A SEMICONDUCTOR, METHODS OF FORMING AN ISOLATION TRENCH IN A SURFACE OF A SILICON WAFER, METHODS OF FORMING AN ISOLATION TRENCH-ISOLATED TRANSISTOR, TRENCH-ISOLATED TRANSISTOR, TRENCH ISOLATION STRUCTURES FORMED IN A SEMICONDUCTOR, MEMORY CELLS AND DRAMS

* * * * *

INVENTORS

KEIJI JONO
HIROKAZU UEDA
HIROYUKI WATANABE

ATTORNEY'S DOCKET NO. KM1-001

METHODS OF FORMING AN ISOLATION TRENCH IN A SEMICONDUCTOR, METHODS OF FORMING AN ISOLATION TRENCH IN A SURFACE OF A SILICON WAFER, METHODS OF FORMING AN ISOLATION TRENCH-ISOLATED TRANSISTOR, TRENCH-ISOLATED TRANSISTOR, TRENCH ISOLATION STRUCTURES FORMED IN A SEMICONDUCTOR, MEMORY CELLS AND DRAMS

TECHNICAL FIELD

The present invention relates to methods of forming an isolation trench in a semiconductor, methods of forming an isolation trench in a surface of a silicon wafer, methods of forming an isolation trench-isolated transistor, trench-isolated transistor, trench isolation structures formed in a semiconductor, memory cells and DRAMs.

BACKGROUND OF THE INVENTION

Field-effect transistors ("FETs") are used in memory structures such as dynamic random access memories ("DRAMs") for controlling access to capacitors used to store charge representing information contained in the memories. In DRAMs, charge leakage effects necessitate periodic refreshing of the information stored in the memory. In turn, refreshing of the DRAM leads to increased power consumption and delays in memory operation. Accordingly, it is desirable to reduce charge leakage effects in DRAMs.

Additionally, it is desirable to minimize the area required for fabrication of the elements of memories such as DRAMs. Electrical isolation of various circuit elements from each other is required. In

turn, electrical isolation requires some of the space used on the DRAM or other integrated circuitry. Various techniques have been developed to reduce the amount of area needed for electrical isolation structures. One technique for providing a high degree of electrical isolation while requiring relatively little space is known as shallow trench isolation.

One source of charge leakage in DRAMs is related to carrier generation-recombination phenomena. In general, lower dopant concentrations tend to reduce this source of charge leakage. However, other concerns tend to determine lower bounds for dopant concentrations.

The FETs used as access transistors determine some of these other concerns. The FETs need to be able to provide a high impedance when they are turned OFF, and a low impedance connection when they are turned ON. DRAMs and other memories use an addressing scheme whereby a wordline that is coupled to many transistor gates is selected, and at the same time a bitline or digitline that is coupled to many transistor drains is also selected. A FET that is located at the intersection of the selected wordline and the selected bitline is turned ON, and that memory cell is accessed. At the same time, many other FETs have a drain voltage due to the drains of these FETs being coupled to the selected bitline. These FETs exhibit some parasitic conductance as a result of the drain voltage. In some types of integrated circuits, a portion of that parasitic conductance is due to corner effects that are an artifact of using Trench isolation techniques

to isolate the FETs from one another and from other circuit elements.

These effects are described in "Subbreakdown Drain Leakage Current in MOSFET" by J. Chen et al., IEEE El. Dev. Lett., Vol. EDL-8, No. 11, Nov. 1987; "Impact Of Shallow Trench Isolation On Reliability Of Buried- And Surface-Channel Sub-μm PFET" by W. Tonti and R. Bolam, IEEE Cat. No. 0-7803-2031, 1995; "Shallow Trench Isolation For Advanced ULSI CMOS Technologies", M. Nandakumar et al.; and "Shallow Trench Isolation Characteristics With High-Density-Plasma Chemical Vapor Deposition Gap-Fill Oxide For Deep-Submicron CMOS Technologies", S.-H. Lee et al., Jpn. J. Appl. Phys., Vol. 37, 1998, pp. 1222-1227, which publications are hereby incorporated herein by reference for their general background teachings.

One method of reducing these parasitic conduction effects is to round the corner where the isolation trench meets the surface of the semiconductor material. This may be effected by oxidizing the surface of the silicon, as is described in the above-noted publications. However, this approach requires additional processing steps, which tend to result in reduced yield, among other things.

What is needed is a way to incorporate trench isolation together with FETs that does not increase processing complexity and that provides compact, low-leakage transistors in DRAMs and other circuitry.

SUMMARY OF THE INVENTION

In one aspect, the present invention provides a method of forming an isolation trench in a semiconductor. The method includes forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle. The method also includes forming a second isolation trench portion within and extending below the first isolation trench portion. The second isolation trench portion has a second depth and includes a second sidewall. The second sidewall intersects the first sidewall at an angle with respect to the surface that is greater than the first angle. A dielectric material fills the first and second isolation trench portions.

In another aspect, the present invention includes a method of forming an isolation trench in a surface of a silicon wafer. The method includes forming a mask on the surface, where the mask includes an opening and sidewalls, and etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67 to form a first isolation trench portion.

In a further aspect, the present invention includes a trench-isolated transistor. The trench-isolated transistor includes first and second isolation trenches each disposed on a respective side of a portion of silicon. The first and second isolation trenches each include a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle. The first and

second isolation trenches each also include a second isolation trench portion within and extending below the first isolation trench portion. The second isolation trench portion has a second depth and includes a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle. The first and second isolation trenches are filled with a dielectric material. The transistor further includes a gate extending across the silicon portion from the first isolation trench to the second isolation trench, and source and drain regions extending between the first and second isolation trench portions and across the silicon portion. The source region is adjacent one side of the gate and the drain region is adjacent another side of the gate that is opposed to the one side.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a simplified plan view of shallow trench isolation structures and a FET, in accordance with an embodiment of the present invention.

Fig. 2 is a simplified side view, in section, taken along section lines 2-2 of Fig. 1, of the shallow trench isolation structures and FET of Fig. 1, in accordance with an embodiment of the present invention.

Fig. 3 is a simplified side view, in section, illustrating formation of a trench isolation structure, in accordance with an embodiment of the present invention.

Fig. 4 is a simplified flow chart of a process for forming the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

Fig. 5 is a simplified schematic diagram of a memory cell that advantageously employs the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

Fig. 6 is a simplified block diagram of a DRAM that advantageously employs the structures of Figs. 1, 2 and 5, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the Progress of Science and useful Arts" (Article 1, Section 8).

Fig. 1 shows trench isolation structures 10 and a FET 12 formed in a semiconductor substrate 13, in accordance with but one preferred embodiment of the present invention. The FET 12 includes a gate G, which may be formed from polysilicon, a source S and a drain D. The trench isolation structures 10 each include a first isolation trench portion 14 having a first depth 16 and having first sidewalls 18 each

intersecting a surface 20 of the semiconductor substrate 13 at a first angle θ_1.

The trench isolation structures 10 also each include a second isolation trench portion 24 within and extending below the first isolation trench portion 14. The second isolation trench portions 24 have a second depth 26 and include second sidewalls 28 each intersecting one of the first sidewalls 18 at a second angle θ_2 with respect to the surface 20 that is greater than the first angle θ_1 to form shoulders 30 at the juncture of the first sidewall 18 and the second sidewall 28.

In one embodiment, the shoulders 30 result in substantial reduction of subthreshold current through the FET 12. In other words, when the FET 12 is OFF, the amount of current that can be induced in the FET 12 by applying voltage to the drain D is greatly reduced.

In one embodiment, the first angle θ_1 is less than about sixty degrees and the second angle θ_2 is eighty degrees or more. In one embodiment, the first angle θ_1 is in a range of from about five degrees to about forty-five degrees. In one embodiment, the first angle θ_1 is in about thirty-five degrees. In one embodiment, the first angle θ_1 is about forty degrees. The concerns addressed in selecting the first angle θ_1 are to select an angle θ_1 providing a shoulder that reduces electrical fields in the subsequently-formed FET 12 and to also select an angle that does not impede subsequent filling of the trench isolation structures 10 with dielectric material such as silicon dioxide.

Further in the illustrated embodiments, substantially straight linear segment 18 extends entirely between and to outermost surface portion 20, respectively, and to segment 28. Substantially straight linear segment 28 extends from segment 18 to a bottom of the trench isolation structure 10.

Alternate embodiments are, of course, contemplated whereby some substantially straight linear segment occurs somewhere within each of first sidewalls 18 and second sidewalls 28, without extending over the entirety of the first 18 and second 28 sidewalls. In the context of this patent, "substantially straight linear" means a perfectly straight segment as well as a segment that has a degree of curvature associated with it. A curved segment is to be considered "substantially straight linear" in the context of this patent provided that it has some chord length greater than or equal to 30 nanometers and has some radius of curvature of at least 20 nanometers.

The first sidewall 18 needs to incorporate a lateral dimension wide enough such that wet dips occurring during processing steps such as nitride hard mask removal and those subsequent up to gate oxide growth do not start to etch down the sidewall of the isolation trench structure 10. That dimension is proportional to the various dielectric layer thicknesses, and so can vary greatly from process to process and through different technology generations. Exemplary minimum extents for

the first sidewalls 18, i.e., distance from the top surface 20 to the shoulder 30, are in a range of from 50 Angstroms to 500 Angstroms.

Fig. 3 is a simplified side view, in section, illustrating formation of a trench isolation structure, in accordance with an embodiment of the present invention. In one embodiment, the trench isolation structures 10 are created by forming a masking layer 32 on the semiconductor surface 20. In one embodiment, the masking layer 32 includes a silicon dioxide layer 34 having a thickness of about 100 Angstroms and a silicon nitride layer 36 having a thickness of about 1000 Angstroms. A photoresist layer 38 is formed on the masking layer 32, and openings 40 corresponding to the trench isolation structures 10 are formed in the photoresist. The openings 40 have sidewalls 42.

In one embodiment, a plasma etch is used to form openings in the masking layer 32. The plasma etch is also used to etch the first isolation trench portions 14. In one embodiment, the plasma etch is performed using a mixture of fluorocarbon and fluorohydrocarbon gases, such as, by way of example, CF_4, CHF_3, CH_2F_2 and/or C_2F_8 or the like. In one embodiment, the plasma etch is performed using a mixture of CF_4 and CHF_3 in a ratio ranging from 0.11 to 0.67.

In one embodiment, the masking layer 32 is etched, and then etching is continued for a predetermined time to etch the first isolation trench portion 14. In one embodiment, the etching is carried out for 30 seconds, where the first half of the etching process is used to broach

the masking layer 32. In one embodiment, the etching is carried out for 40 seconds. A broad variety of implementations are possible, using different etch gas compositions, pressures and etch times, as may be seen by comparing these examples to the example below. In one embodiment, etching is carried out using parameters given below in Table I in a Hitachi microwave etcher model 511A, using the photoresist 38, silicon nitride 36 and silicon dioxide 34 mask structure 32 described above.

TABLE I

EXEMPLARY SHOULDER FORMATION PROCESSING PARAMETERS

Parameter	Units	Mask etch	Overetch	Trench	De-chuck
Step time	seconds	60	22	78	1.0
Gas 1	sccm	200	200	0	150
Gas 2	sccm	160	60	0	0
Gas 3	sccm	40	140	0	0
Gas 4	sccm	0	0	100	0
Gas 5	sccm	0	0	5.7	0
Pressure	mTorr	20	20	6	7.5
Power 1	W	550	550	800	1000
Power 2	W	90	130	60	0

Notes: gas 1 corresponds to argon, gas 2 corresponds to CF_4, gas 3 corresponds to CHF_3, gas 4 corresponds to HBr, gas 5 corresponds to O_2, power 1 corresponds to magnetron power and power 2 corresponds to applied RF power.

The shoulder 30 is formed by a process whereby a polymer 44 is formed on the sidewalls 42. By adjusting the composition of the etching gases, applied RF power, chamber pressure and the like, the polymer 44 is formed at a rate that encourages a particular first angle θ_1 to be formed during the etching process. By stopping the etching and polymer deposition at the end of the predetermined time interval, the first

depth 16 can be controlled. The second isolation trench portion 24 is then etched, using a different etch gas mixture, for example, as noted in Table I.

In another embodiment, a first etch is carried out to provide the first isolation trench portion 14. A second masking step is then carried out, and openings corresponding to the second isolation trench portion 24 are created. The second isolation trench portion 24 is then etched.

In one embodiment, the first depth 16 is chosen to be five to thirty or fifty percent of the total trench depth, i.e., the first depth 16 plus the second depth 26. In one embodiment, the first depth 16 is chosen to be five to fifteen percent of the total trench depth. In one embodiment, bottoms of the trenches are implanted with dopant after the first 14 and second 24 trench portions are etched. This allows a shallower trench to be employed, and results in the first depth 16 being a larger percentage of the total trench depth.

In one embodiment, implant doses required to form the source S and drain D regions are reduced by as much as ten percent when the shoulder 30 is present, resulting in an increase of as much as thirty percent of the time required between refresh cycles. For example, if a typical implant dose of $5.4 \times 10^{12}/cm^2$ were ordinarily required to dope channel regions, a dose of $4.9 \times 10^{12}/cm^2$ could be employed together with formation of the shoulder 30.

Following etching of the first 14 and second 24 isolation trench portions, the photoresist layer 38 and the polymer 44 may be stripped using a conventional oxygen ashing process. A dielectric material, typically silicon dioxide, may be used to fill the first 14 and second 24 isolation trench portions, and conventional chemical-mechanical polishing may be used to planarize the resultant structure. In one embodiment, plasma etchback is employed to planarize the dielectric material, usually together with another patterning step or a planarizing coating layer. The gate G may be formed using conventional polysilicon, polycide or metal, and the source S and drain D may be formed using conventional ion implantation techniques or doping outdiffusion from subsequent layers.

Fig. 4 is a simplified flow chart of a process P1 for forming the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

In a step S1, the first isolation trench portions 14 are formed. In one embodiment, the first isolation trench portions 14 are formed by forming the masking layer 32, followed by plasma etching, as described above.

In a step S2, the second isolation trench portions 24 are formed. In one embodiment, the second isolation trench portions 24 are formed by etching as described above with reference to Fig. 3 and Table I. In one embodiment, the second isolation trench portions 24 are formed by separate masking and etching operations.

In a step S3, the first 14 and second 24 trench portions are filled with a dielectric using conventional processing techniques as described above. The step S3 may include planarization of the dielectric material, for example via conventional chemical-mechanical polishing.

In a step S4, the FET 12 is formed, using conventional processing techniques, as discussed above. The process P1 then ends, and processing continues using conventional processing operations.

Fig. 5 is a simplified schematic diagram of a memory cell 50 that advantageously employs the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention. The memory cell 50 includes the FET 12 of Figs. 1 and 2, a capacitor 52 coupled to the source S of the FET 12, a wordline 54 coupled to the gate G (and to other gates in other memory cells) and a bitline 56 coupled to the drain D of the FET 12 (and to other drains in other memory cells). By selecting the wordline 54 and the bitline 56, the FET 12 is turned ON, and charge stored in the capacitor 52 can then be measured to determine the datum stored in the memory cell 50. Alternatively, by selecting and turning the FET 12 ON, charge can be injected into the capacitor 52 to write a datum therein, and the FET 12 can then be turned OFF to store the datum in the memory cell 50.

Fig. 6 is a simplified block diagram of a DRAM 60 that advantageously employs the structures of Figs. 1, 2 and 5, in accordance with an embodiment of the present invention. The DRAM 60 includes

a memory cell array 62 coupled to a group of wordlines 56 and a group of bitlines 54. Address decoders, such as a row decoder 64 and a column decoder 68, decode addresses provided via a bus, allowing data to be read from or written to memory cells 50 in the memory cell array 62.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material.

2. The method of claim 1, wherein forming a second isolation trench portion includes forming the second angle to be between eighty and ninety degrees.

3. The method of claim 1, wherein forming a first isolation trench portion includes forming the first angle to be in a range of from about thirty degrees to about seventy degrees and forming a second isolation trench portion includes forming the second angle to be more than eighty degrees.

4. The method of claim 1, wherein forming an isolation trench in a semiconductor comprises forming an isolation trench in silicon.

5. The method of claim 1, wherein forming a first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls;

continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined time interval.

6. The method of claim 5, wherein etching and depositing comprises:

providing a mixture of gasses chosen from a group consisting of CF_4, CHF_3, CH_2F_2 and C_2F_8; and

supplying radio frequency excitation to the mixture.

7. The method of claim 5, wherein etching and depositing comprises:

providing fluorocarbon gases; and

supplying radio frequency excitation to the mixture.

8. The method of claim 1, wherein forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

9. The method of claim 1, wherein forming the first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67;

depositing a polymer on the sidewalls during plasma etching;

continuing etching for a predetermined time after the silicon nitride layer has been broached and continuing depositing polymer on the sidewalls; and

stopping etching and depositing when the predetermined interval ends.

10. The method of claim 1, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

11. The method of claim 1, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

12. The method of claim 1, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

13. A method of forming an isolation trench in a surface of a silicon wafer comprising:

forming a mask on the surface, the mask including an opening and sidewalls; and

etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67 to form a first isolation trench portion.

14. The method of claim 13, wherein etching the silicon surface includes forming a first isolation trench portion having a first sidewall that intersects the silicon surface at an angle in a range of from about thirty degrees to about seventy degrees.

15. The method of claim 14, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

16. The method of claim 13, further comprising forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle.

17. The method of claim 16, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

18. The method of claim 17, further comprising:

filling the first and second isolation trench portions with dielectric material; and

planarizing the dielectric material filling the first and second isolation trench portions.

19. The method of claim 13, wherein forming a mask comprises:

forming a silicon nitride layer on the semiconductor surface; and

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

20. The method of claim 19, wherein etching the surface comprises:

plasma etching through the silicon nitride layer;

continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined time interval.

21. The method of claim 19, further comprising forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle.

22. A method of forming an isolation trench-isolated transistor comprising:

forming first and second isolation trenches disposed to a respective side of a portion of silicon, forming the first and second isolation trenches comprising:

forming a mask on the surface, the mask including first and second openings corresponding to the first and second isolation trenches;

forming a first isolation trench portion in each of the first and second openings, each first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and

forming a second isolation trench portion within and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater than the first angle; the method further comprising:

filling the first and second isolation trench portions with dielectric material;

forming a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions extending between the first and

second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

23. The method of claim 22, wherein forming a first isolation trench portion comprises etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

24. The method of claim 22, wherein forming a mask comprises:

forming a silicon nitride layer on the semiconductor surface; and

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

25. The method of claim 22, wherein forming a first isolation trench portion comprises:

plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls;

continuing etching for a predetermined time after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined interval.

26. The method of claim 25, wherein plasma etching comprises etching using gases including CF_4 and CHF_3 in a ratio of $CF_4/CHF_3 = 0.11$ to 0.67.

27. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first sidewall intersecting a surface of the semiconductor at an angle in a range of from about thirty degrees to about seventy degrees.

28. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

29. The method of claim 27, wherein forming a second isolation trench portion comprises forming a second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface.

30. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

31. The method of claim 30, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

32. The method of claim 22, wherein forming a gate comprises forming a gate comprising polysilicon.

33. A trench-isolated transistor comprising:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions, the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

34. The trench-isolated transistor of claim 33, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

35. The trench-isolated transistor of claim 33, wherein the second angle is between eighty and ninety degrees.

36. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

37. The trench-isolated transistor of claim 33, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

38. The trench-isolated transistor of claim 33, wherein the dielectric material filling the first and second isolation trench portions has a planar surface.

39. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

40. The trench-isolated transistor of claim 39, wherein the second angle is in a range of from eighty to ninety degrees.

41. The trench-isolated transistor of claim 33, wherein the transistor is formed as a part of a memory integrated circuit.

42. A trench isolation structure formed in a semiconductor comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions.

43. The trench isolation structure of claim 42, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

44. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

45. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

46. The trench isolation structure of claim 42, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

47. The trench isolation structure of claim 42, wherein the trench isolation structure is formed in a memory integrated circuit.

48. A memory cell including:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the

source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

49. The memory cell of claim 48, wherein the gate comprises polysilicon.

50. The memory cell of claim 48, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

51. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

52. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

53. The memory cell of claim 48, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

54. The memory cell of claim 48, wherein the memory cell is included within a DRAM integrated circuit.

55. A DRAM comprising:

address decoding circuitry;

a group of bitlines coupled to the address decoding circuitry and extending in a first direction;

a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection;

a plurality of memory cells each disposed at one of the intersections, each memory cell comprising:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second

sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

each memory cell further including:

one bitline of the group of bitlines coupled to the drain; and

one wordline of the group of wordlines coupled to the gate.

56. The DRAM of claim 55, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

57. The DRAM of claim 55, wherein the gate comprises polysilicon.

58. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

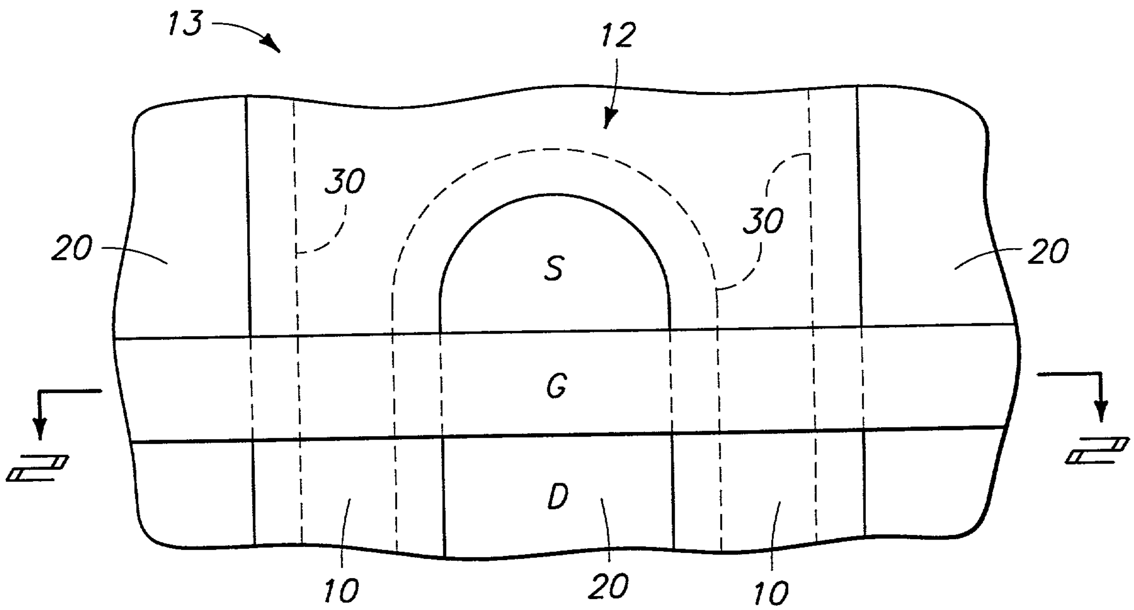
59. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

60. The DRAM of claim 55, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

61. The DRAM of claim 55, wherein the dielectric material filling the first and second isolation trench portions includes a planar outer surface.

ABSTRACT OF THE DISCLOSURE

A method of forming an isolation trench in a semiconductor includes forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle. The method also includes forming a second isolation trench portion within and extending below the first isolation trench portion. The second isolation trench portion has a second depth and includes a second sidewall. The second sidewall intersects the first sidewall at an angle with respect to the surface that is greater than the first angle. A dielectric material fills the first and second isolation trench portions.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S
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G
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D
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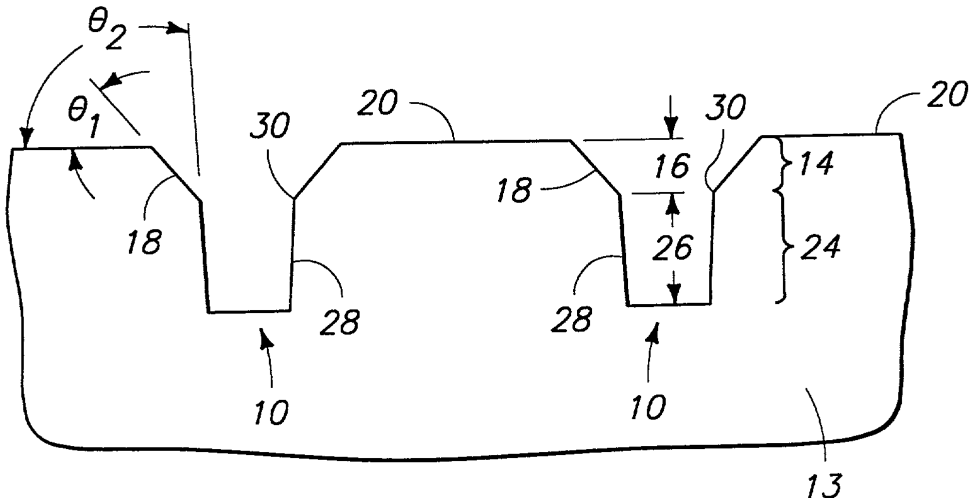
20
10

Fig 1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θ1
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18
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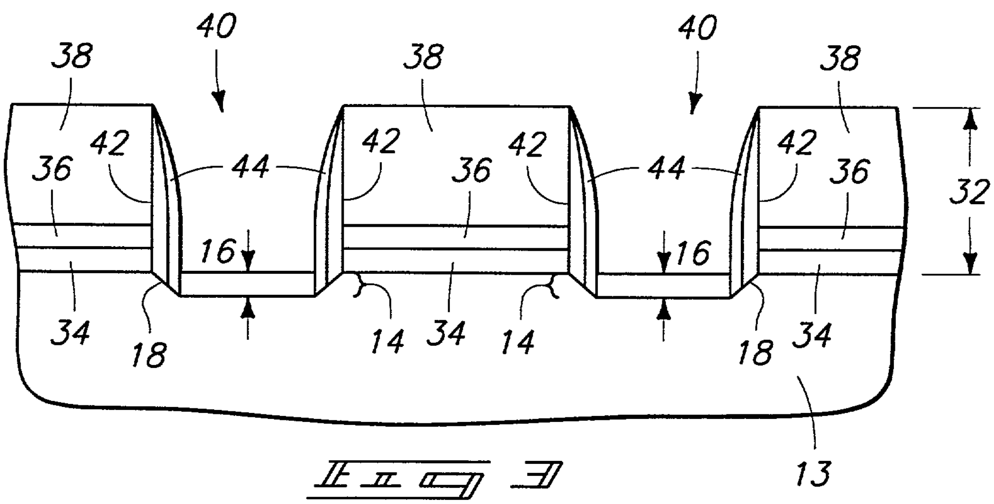
10
13

Fig 2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18
14
32
13

Fig. 3

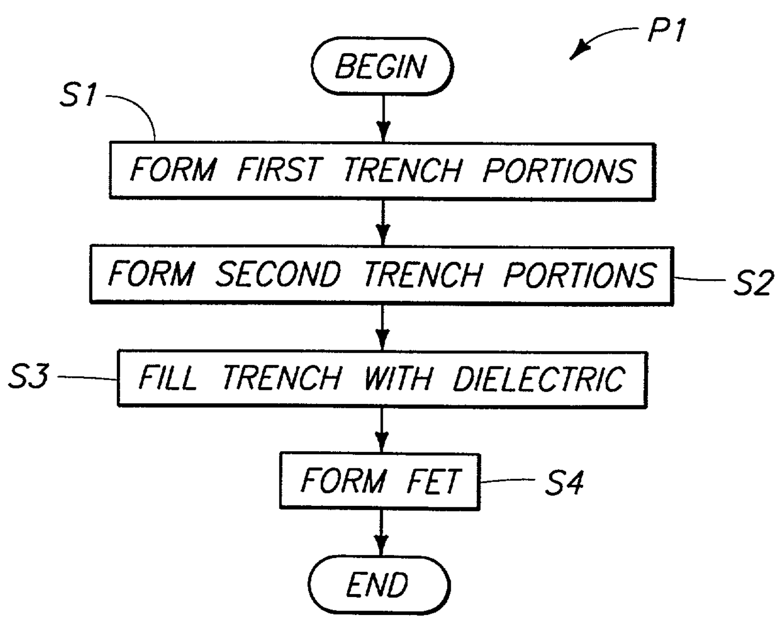
P1
BEGIN
S1
FORM FIRST TRENCH PORTIONS
FORM SECOND TRENCH PORTIONS
S2
S3
FILL TRENCH WITH DIELECTRIC
FORM FET
S4
END

Fig. 4

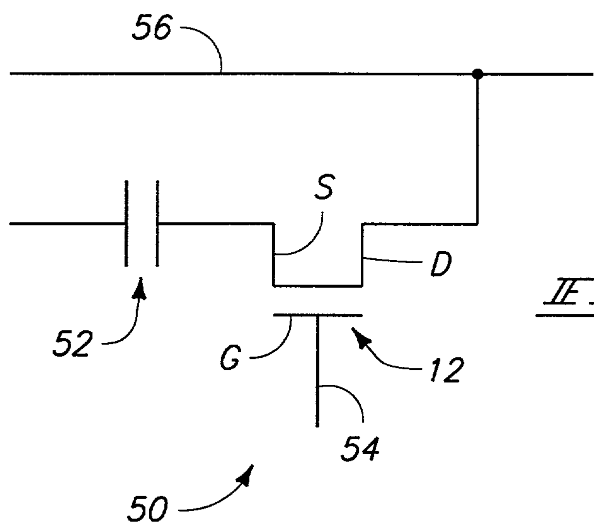
56
S
D
52
G
12
54
50

Fig 5

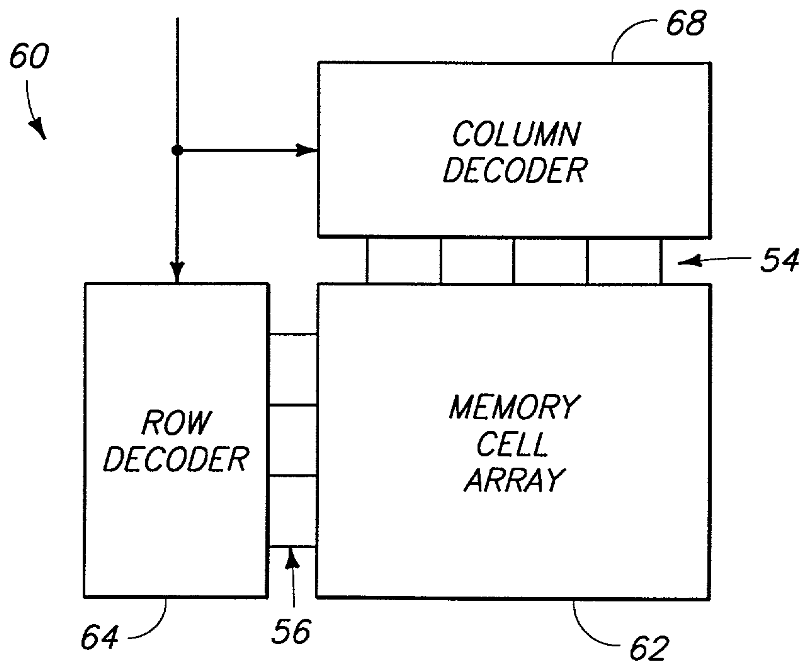
60
68
COLUMN DECODER
54
ROW DECODER
MEMORY CELL ARRAY
64
56
62

Fig 6